A SOLID-STATE PROGRAMMABLE DIGITAL CLOCK

by

S. Chalasani and B. J. Flaherty

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Sponsored by

National Aeronautics and Space Administration

Washington 28, D.C.

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Technical Report No. 30

Ionosphere Radio Laboratory

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LIST OF ILLUSTRATIONS

ABSTRACT

Laboratories such as those engaged in recording data from satellites have long felt the need for a special purpose, programmable, accurate and reliable digital clock to automatically record their data at preset times. Such a solid-state digital clock has been designed and actually constructed to have four ON settings. When the preset ON time coincides with the indicated time, the clock outputs a 4.5 volt pulse of one minute duration to operate the recording equipment. A separate timing motor determines the duration of the data recording. The clock has been built with a 200 KHz oscillator (long term stability $\pm 1 \times 10^{-6}$ per day), integrated circuit decade dividers, decoders, NAND gates, transistorized AND gates, flip-flops, etc. It has been shown how the design can be extended to include four corresponding OFF settings to control the duration of the recording time. It has also been shown that, theoretically, the ON settings on the clock can be increased to a maximum of 60 or alternately a clock with 30 ON settings and 30 OFF settings.

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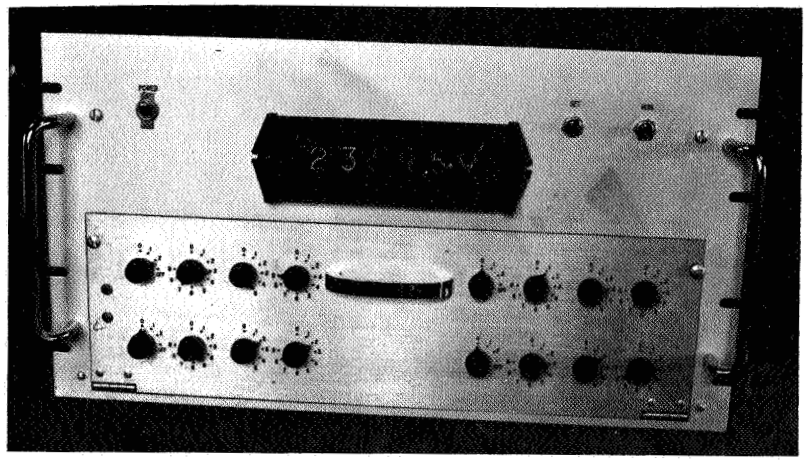
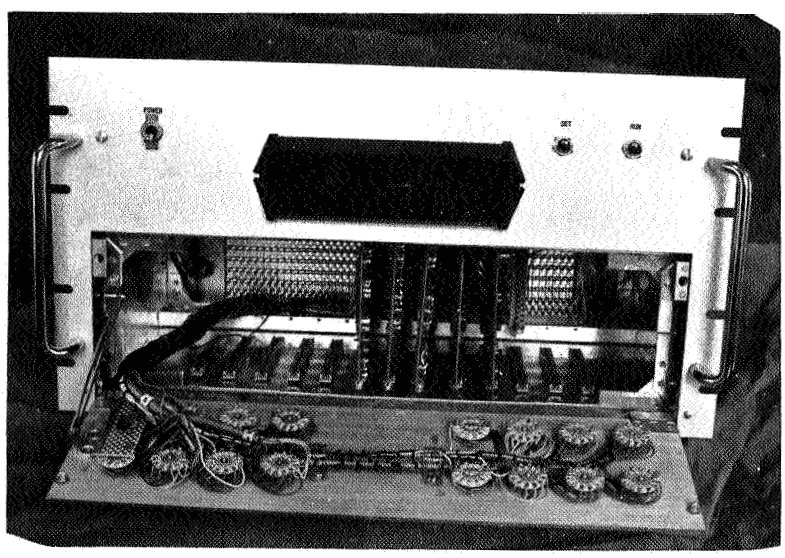


10A - 11 Programable digital clock indicating 23 hours 59 minutes and 59 seconds.



7A - 8 Programable digital clock with front panel open for access to circuit cards.

I. INTRODUCTION

In most systems which collect data or record events, it is desirable to have a general purpose clock from which the real time of day may be read or outputed. The clock also should be able to start and stop recording the data at a number of previously preset times during a day. The object of this project is to design and build a reliable electronic clock, to indicate the time of the day up to a second and to have four presettings. When the clock's time coincides with one of the four preset times, a pulse of one minute duration is outputed from the instrument. The instrument is built specifically to operate the satellite data recording equipment at the Geophysical Observatory at the University of Illinois, but its capability is more extensive.

Electronic clocks may be divided into five classes: (1) those in which an impulse is given directly to a pendulum or balance, (2) those in which an escapement or pendulum is driven by a spring or weight alternately liberated and wound electrically, (3) those driven by alternating current synchronous motors, (4) quartz crystal clocks and (5) atomic clocks.

Since the first two are no longer being used, they are of historical importance only. Synchronous motor clocks are being used where accuracy and reliability are not very important because of their dependence on the supply frequency. Crystal clocks are used mainly as secondary standards in laboratories; their stability approaches $\pm 1 \times 10^{-10}$ per 24 hours (Hewlett-Packard, 1967). Atomic clocks are used as primary standards. They are expensive and complicated with a stability $\pm 1 \times 10^{-11}$ per 24 hours.

..1 Synchronous Motor Clocks (Wise, 1948)

Synchronous motor clocks have a steel rotor, The steel chosen has appreciable magnetic hysterisis. The rotor as mounted between the poles of an electro-magnet energized from the alternating current supply. The direction of the E.M.F. is reversed twice in every cycle. As the current changes, the magnetic flux changes. The rotor of the synchronous motor follows faithfully these changes. If it is a two-pole motor, the rotor completes half a revolution at the first positive half of the wave and the remaining half revolution in the negative half of the wave. Hence, the speed is 60 × 60 = 3600 rpm (for 60 c/s supply) due to the magnetizing and demagnetizing of the alternating field of the embracing stator poles. In general the synchronous speed of a motor is $\frac{120f}{p}$ where f is the supply frequency in Hz and p is the number of poles. The synchronous speed of the motor is then geared down to the required speed by worm and pinion drive to run the time indicators. The main disadvantage of using the synchronous motor clock as a standard is its dependence on supply frequency. Usually the clock is run from the A.C. mains whose supply frequency may vary from 58 cps to 62 cps, and hence the indication time would vary.

The clock, now in operation at the Geophysical Observatory at the University of Illinois, uses transistorized flip-flops to count down from 15360 Hz (crystal oscillator) to 60 Hz which feeds a synchronous motor through a power amplifier. The synchronous motor rotates a constant 3600 rpm which is geared down to 1 rpm and drives a cam mechanism. The cam mechanism sends out one pulse for each revolution. This pulse, in turn, steps a series of stepping switches. The major disadvantage of this clock is the use of relay stepping switches since they are not reliable.

With the advent of the semiconductor, the use of a transistor as a switch is found to be more reliable than the rePay. This can be seen by comparing their performances as switches in the following table (see also Figure 1).

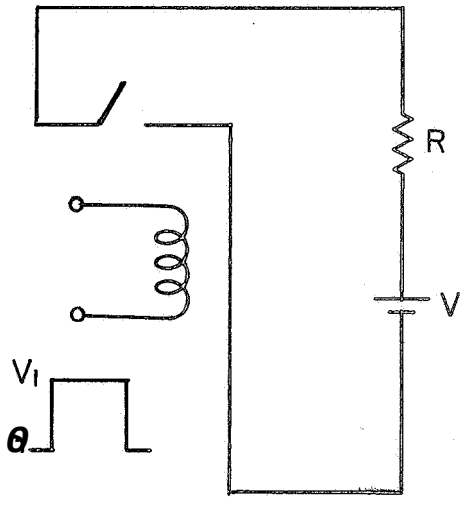
Table 1 - Performance of Relay vs Transistor

	Relay	Transistor
1. Moving parts	Mot reliable as it has moving parts that are subject to wear.	More reliable as it has no moving parts and therefore lacks mechanical contacts that are subject to wear.
2. Speed of operation	Slow by a factor of more than 1000 when compared to transistor.	Operating time is reduced by factor of more than 1000 compared to relay.
3. Noise	Radiates noise in the RF spectrum which can interfere with other systems.	No such noise.
4. Ratio of open to closed circuit resistance introduced into the load circuit.	Superior to transistor as it approaches infinity.	Finite collector emitter resistance when full ON and leakage current when full OFF make it inferior to relay. This is not serious in a properly designed circuit.

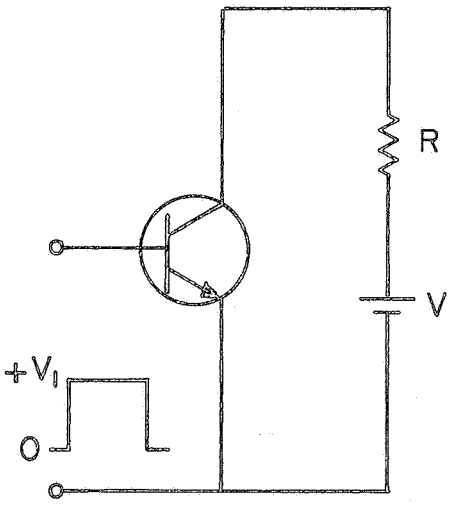
Besides the drawbacks of the stepping switches, the clock at the Geophysical Observatory becomes more complex as one increases the number of presettings to more than two.

1.2 Crystal Clocks

In crystal clocks a crystal controlled oscillator serves as the basic timing source. Crystals achieve a greater degree of stability and accuracy



a) RELAY AS A SWITCH



b) TRANSISTOR AS A SWITCH

Figure 1. Transistor vs Relay

at relatively high frequency. An accuracy of one part in 10^8 can easily be achieved (Irwin and Jensen, 1966). The high source frequency is electronically divided, usually by decade dividers, to the required frequency. A decade divider divides the input frequency by a factor of ten. In the past tubes and then transistors were used to build decade dividers, Since the advent of integrated circuits, integrated circuit decade dividers have been replacing other forms of decade dividers because they are inexpensive, very small in size and reliable over limited temperature and voltage ranges (Khambata, 1965).

The use of integrated decade counters drastically reduces the actual number of elements needed for the clock's implementation, e.g., only five packages are needed to divide down from 100 KHz to 1 Hz. Both active and passive circuit components in the divider are formed in the bulk material and become an indivisible and unalterable part of this material, Interconnection between various components are obtained by deposition of conductors by thin-film technology or in some cases by ingenious juxtaposition of some of the components within the bulk material itself, Input/output connections are made by bonding thin wire leads to selected points on the surface of the semiconductor slice representing the required nodal points of the particular circuit configuration.

The advantages of using integrated circuits compared to other electronic circuits are as follows:

1. Increased Reliability

   In the past electrical connections have been one of the largest factors contributing to reliability of electronic equipment. In integrated circuits the number of point connections of conventional

type are reduced. The connections between circuit components on a silicon block are made by deposited interconnecting patterns and are inherently more reliable than individual discrete connections.

2. Increased Speed of Operation

The physical size of a system directly limits its operating sped because of propagation delay. Integrated circuits increase the speed of operation since all the components are formed in the bulk material and are closely interconnected.

3. Space

Integrated circuits occupy less space.

4. Cost

Initially, integrated circuits were expensive but as the processes improved, higher yields brought costs down. Currently, the price of integrated circuits compares favorably with other types of circuits.

5. Serviceability and Maintenance

It is impossible to replace a defective component in an integrated circuit, The entire circuit must be treated as a single component, If a component is faulty, the entire circuit must be replaced by a known good component circuit.

As the main purpose of this project was to build a reliable clock, integrated circuit decade counters, decoders and gates were used in its construction.

II. DESIGN SPECIFICATIONS

The following are the design specifications to which the clock was built.

1. Count Input

   a) Input Frequency 100 KHz

      Width of count input pulse $\geq$ 50 ns

      Width of reset pulse $\geq$ 50 ns

      Count advances from logic 1 to logic 0

   b) Logic 1 Requirements

      Voltage: Maximum 5.5v

      Minimum 2.2v

      Current: Maximum 1 mA

      Minimum 80 μA

   c) Logic 0 Requirements

      Voltage: Maximum + 0.6v DC

      Minimum - 0.6v DC

      Current: Maximum 3.2 mA

2. Power Supply Voltages and Currents

	Voltage	Current
a)	4.75 to 5.25v DC	1 amp (nominal)
b)	- 6v DC $\pm$ 10%	25 mA (nominal)
c)	200v DC $\pm$ 10%	25 mA (nominal)

3. BCD Output of Counters

   Code 1-2-4-8

4. Temperature

   Operating 0° C to 70° C

5. output Specifications

a) 4.5v pulse for one minute duration at preset time.

b) Number of presettings at a time is four.

III. LOGIC DESIGN

According to the design specifications, the clock has to meet certain logic requirements, The first requirement is that the clock be provided with four presettings. When the preset time coincides with the clock's indicated time, a pulse of one minute duration is to be outputed. This can be accomplished by the incorporation of the logic discussed in III.1. In Section III.2 it is shown how the design may be extended to include four corresponding OFF settings to have control over the duration of recording time, The logic designs for automatic change of time from 2359:59 to 0000:00 and for the setting of the clock are discussed in III.3 and III.4, respectively.

III.1 Preset Logic for ON Settings Only (McCluskey, 1965 and Digital Logic Handbook, 1966)

Let W represent 1/10 hours counter,

X represent 1 hour counter,

Y represent 1/10 minutes counter,

Z represent 1 minute counter,

U represent 1/10 seconds counter, and

V represent 1 second counter.

Let $W^iX^iY^iZ^i$ represent the preset time for the ith presetting or ON setting. Since four ON settings are required, i = 1, 2, 3, and 4, Let the coincidence between the preset time and the indicated time be represented by logic 1 and the not-coincidence by logic 0. At the ith coincidence, $W^iX^iY^iZ^i = 1$; that is, $W^i = X^i = Y^i = Z^i = 1$.

Since any Boolean function can be expanded by a canonical sum, we may write f as

$$f = W^1X^1Y^1Z^1 + W^2X^2Y^2Z^2 + W^3X^3Y^3Z^3 + W^4X^4Y^4Z^4$$

$$= f_1 + f_2 + f_3 + f_4 \qquad (1)$$

Thus f is a minimal sum where f_1, f_2, f_3 and f_4 represent the first, second, third and fourth ON setting times, When f_i is one (outputs a pulse), the ith ON setting coincides with the indicated time, and when f_i is zero (no output pulse or ground potential), the ON setting does not coincide with the indicated time. The network shown in Figure 2 using AND and OR gates is one way to realize the function f given by Equation 1.

Another way of realizing f is based on rewriting f using De Morgan's Theorem:

$$f = f_1 + f_2 + f_3 + f_4 = \overline{(\bar{f}_1\bar{f}_2\bar{f}_3\bar{f}_4)} \qquad (2)$$

where $\bar{f}_i = \overline{(w^i x^i y^i z^i)}$ and the bar indicates the complement. The realization of f using NAND gates is shown in Figure 3. This is the logic that was used in the clock's construction.

III.2 ON and OFF Settings

The logic in the previous section can be extended to include OFF settings. Instead of having an output pulse of one minute duration for each ON setting, the duration of output pulse for each ON setting can be controlled to the desired duration by including an OFF setting; that is, when the OFF setting coincides with the indicated time of the clock, the output pulse ceases to exist. To do this, one must introduce a memory into the logic circuitry; an R-S flip-flop serves this function (Figure 4 is the block diagram).

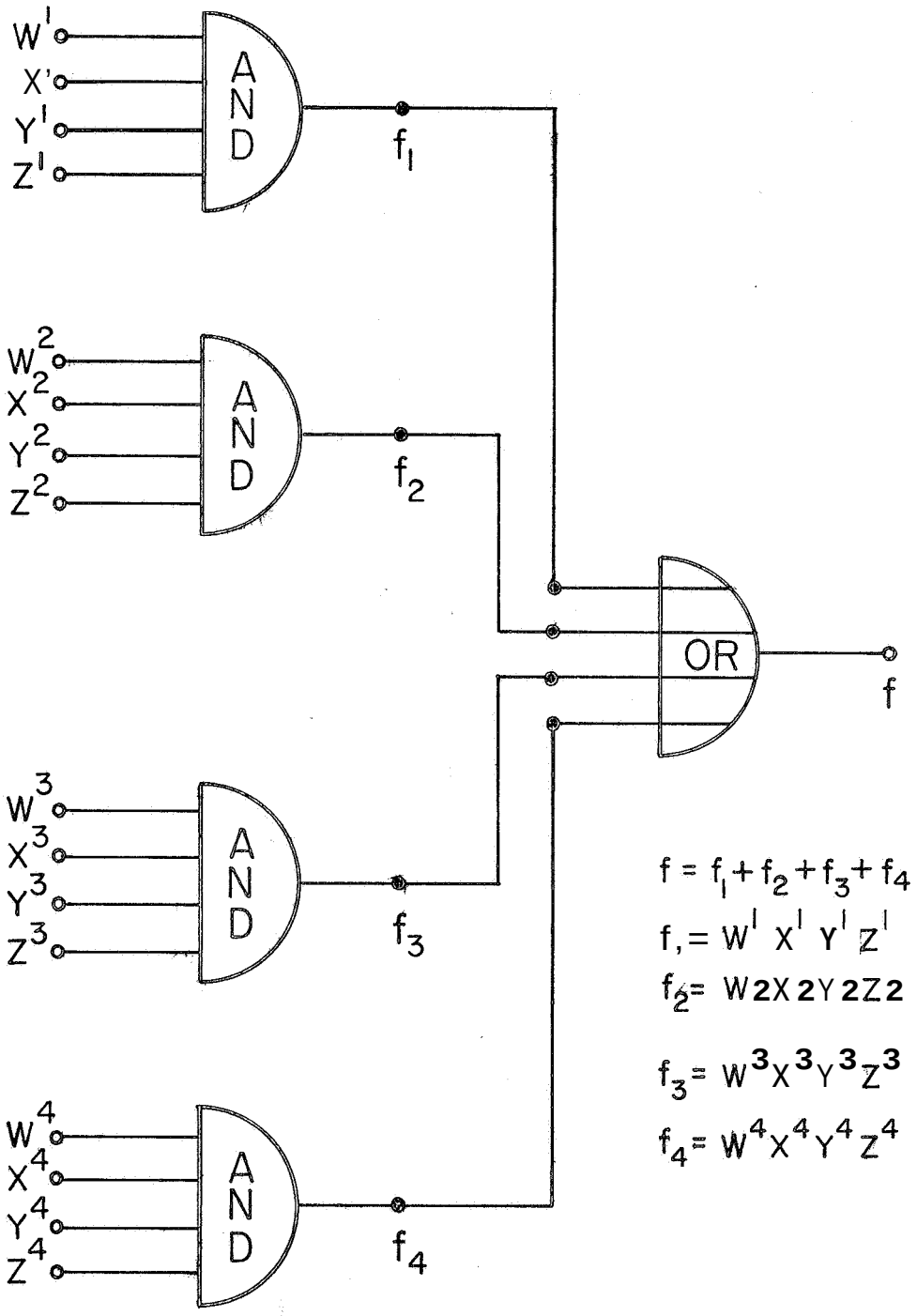


Figure 2. Realization of f Using AND and OR Gates

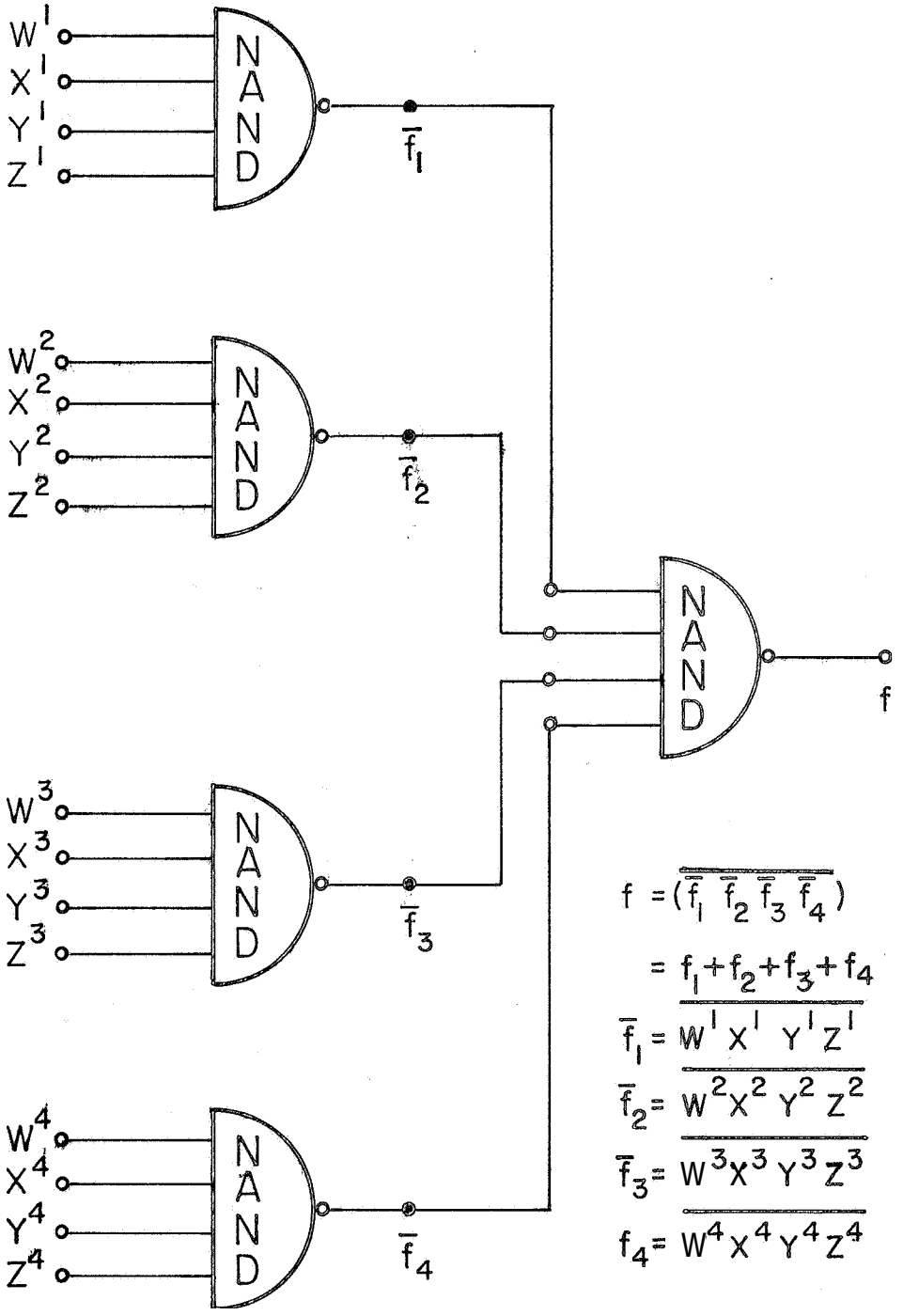


Figure **3. Realization of f** Using NAND Gates

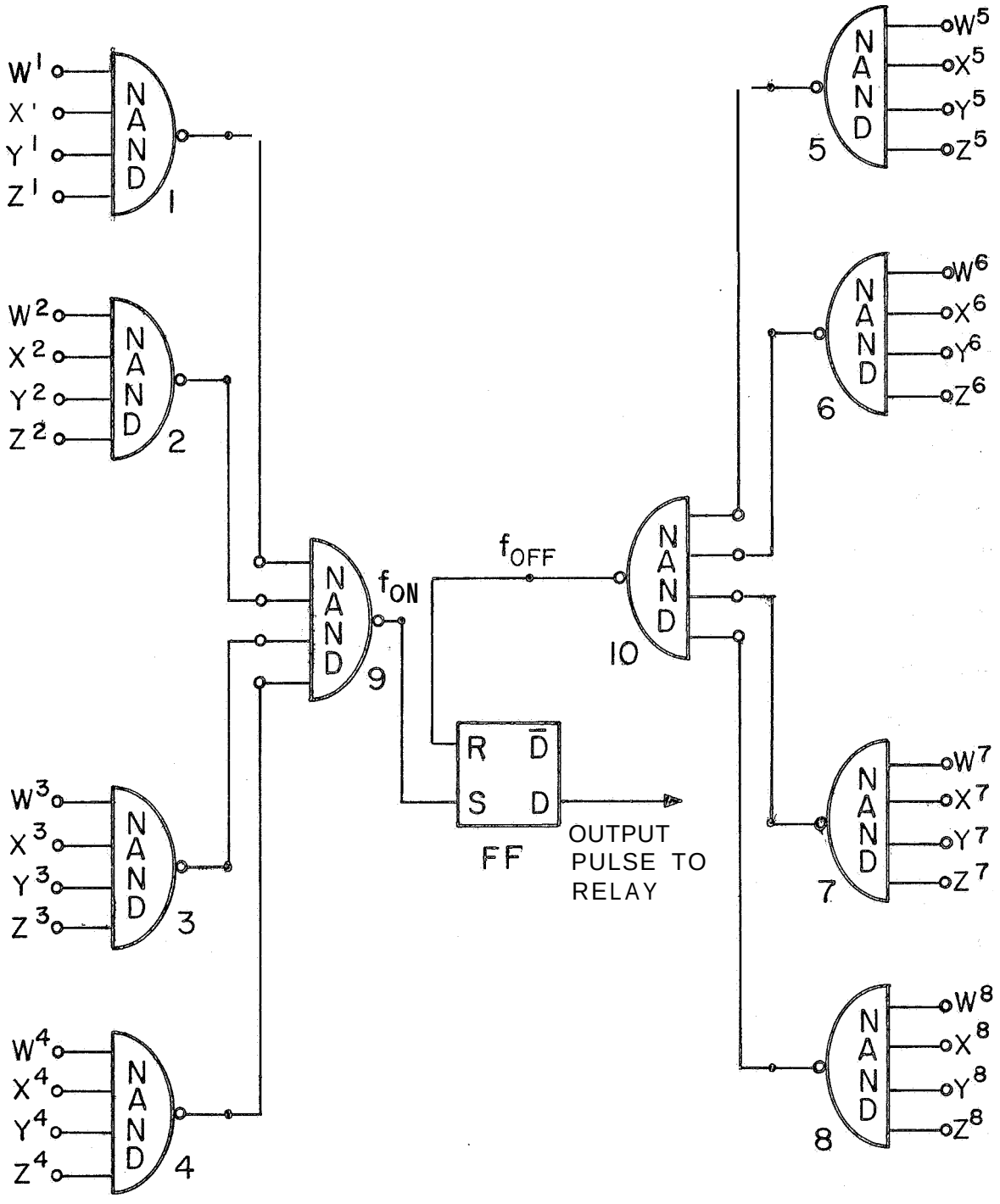


Figure 4, Preset Logic (for both ON and OFF settings)

ON and OFF settings must occur alternately and at the ith ON setting; the output of **NAND** gate nine (f_{ON}) is one. The outputs f_{ON} and f_{OFF} (output Of **NAND** gate ten corresponding to the ith OFF setting] are fed to the *S* and R inputs of a S-R flip-flop. The output pulse f_{ON} changes the state of the FF from zero to one which starts the data recorder, At the ith OFF setting, f_{OFF} becomes one and the state of the FF changes from one to zero **to** stop the recorder.

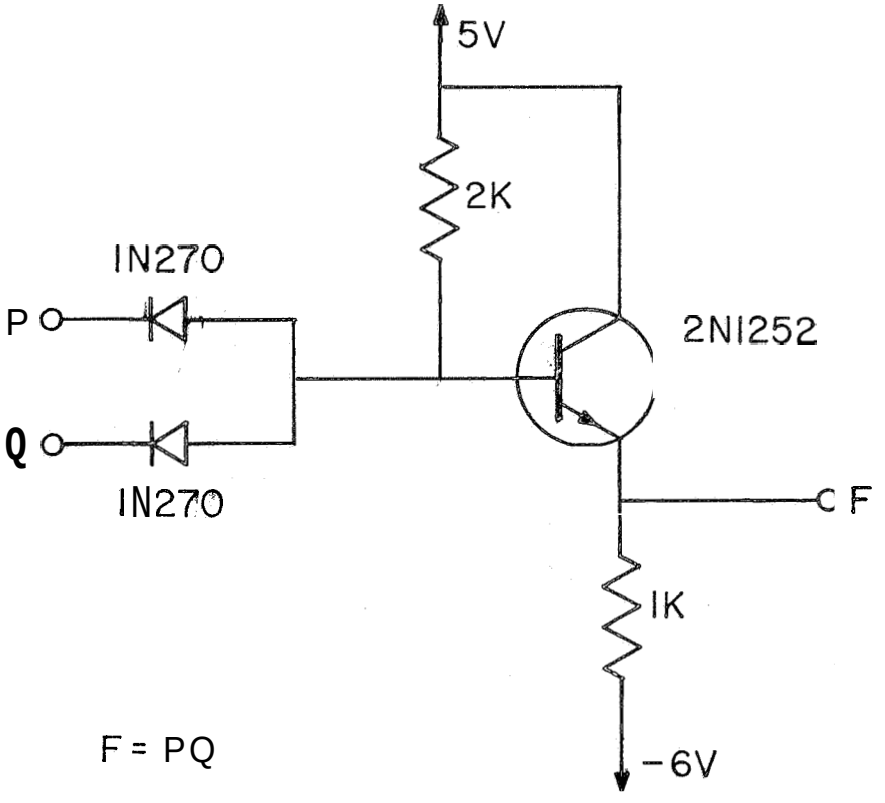
III.3 Logic for Automatic Change of Time from 2359:59 to 0000:00

The clock should automatically change to 0000:00 after 2359:59 without 2400:00 being indicated. This is accomplished by using an AND gate shown in Figure *5*. **P** and Q are the input terminals and F is the output terminal of the **AND** gate. **P** is connected to the decimal output 2 of the decoder of counter W, Q is connected to the decimal output 4 of the decoder of counter X and F is connected to the reset Pines w and x of the counters W and X. When the indicated time changes from 2359:59 to 2400:00, F becomes 1 and sets the counters W and X to 0. There is a time delay of about 40n secs (time delay of AND gate and counters W and X) for the counters to change from 2400:00 to 0000:00. The nixie indicators cannot respond during this brief time and! one can see only the time changing from 2359:59 to 0000:00.

III.4 Setting of Clock

The clock can be set to any time using flip-flops, AND and OR gates. The logic is shown in Figure 6, and the circuit diagram of the flip-flop is shown in Figure 7. Setting the clock is accomplished in the following steps:

1. Set the switches corresponding to the first ON setting of the desired time. (This should be done about one minute ahead of the desired set time,]



P is connected to the decimal output 2 of the decoder of counter W
Q is connected to the decimal output 4 of the decoder of counter X
F is connected to the reset lines of counters W and X

Figure 5, Automatic Change of **Time** from 2359:59 to 0000:00

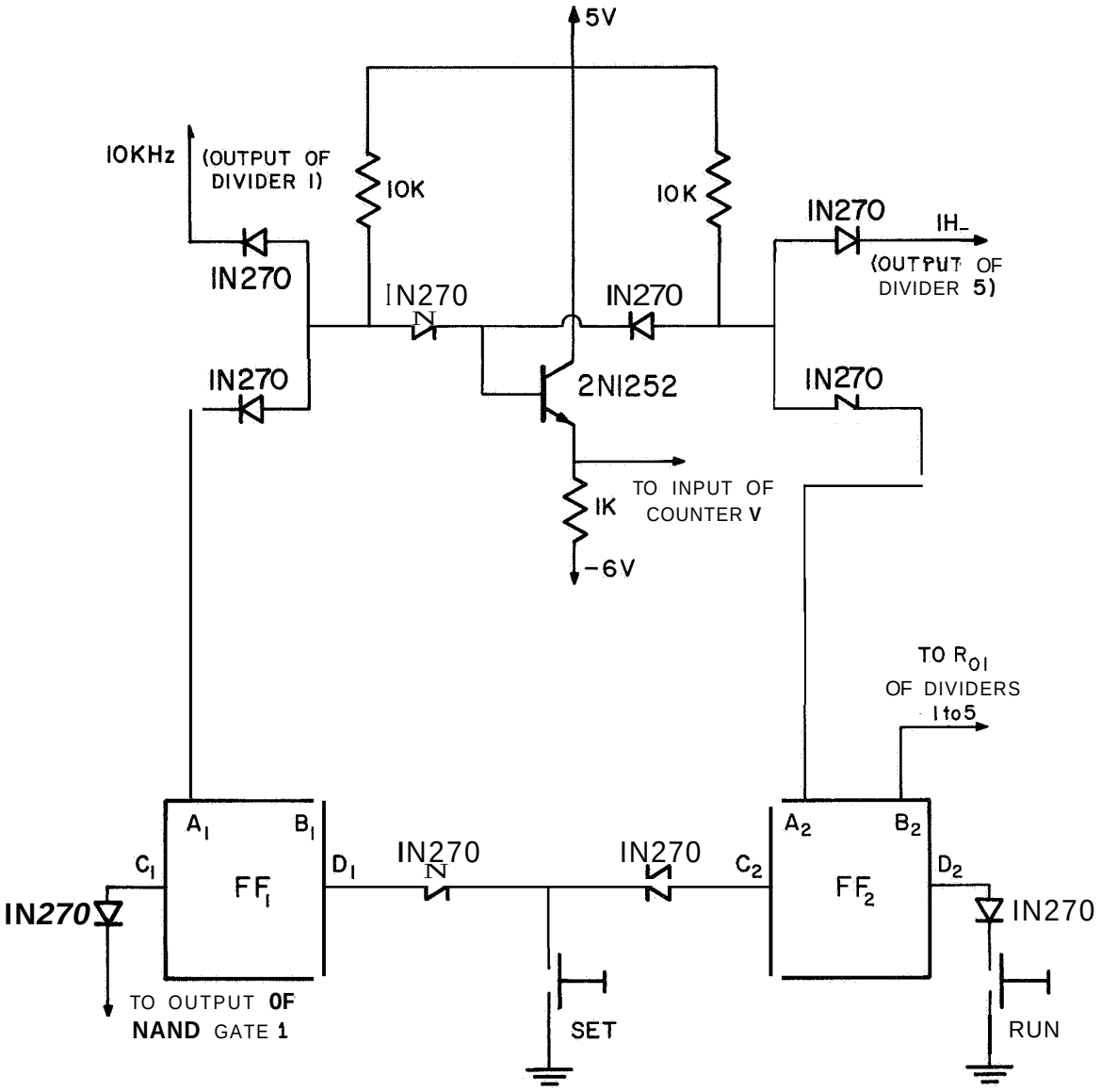


Figure 6. Setting of Clock

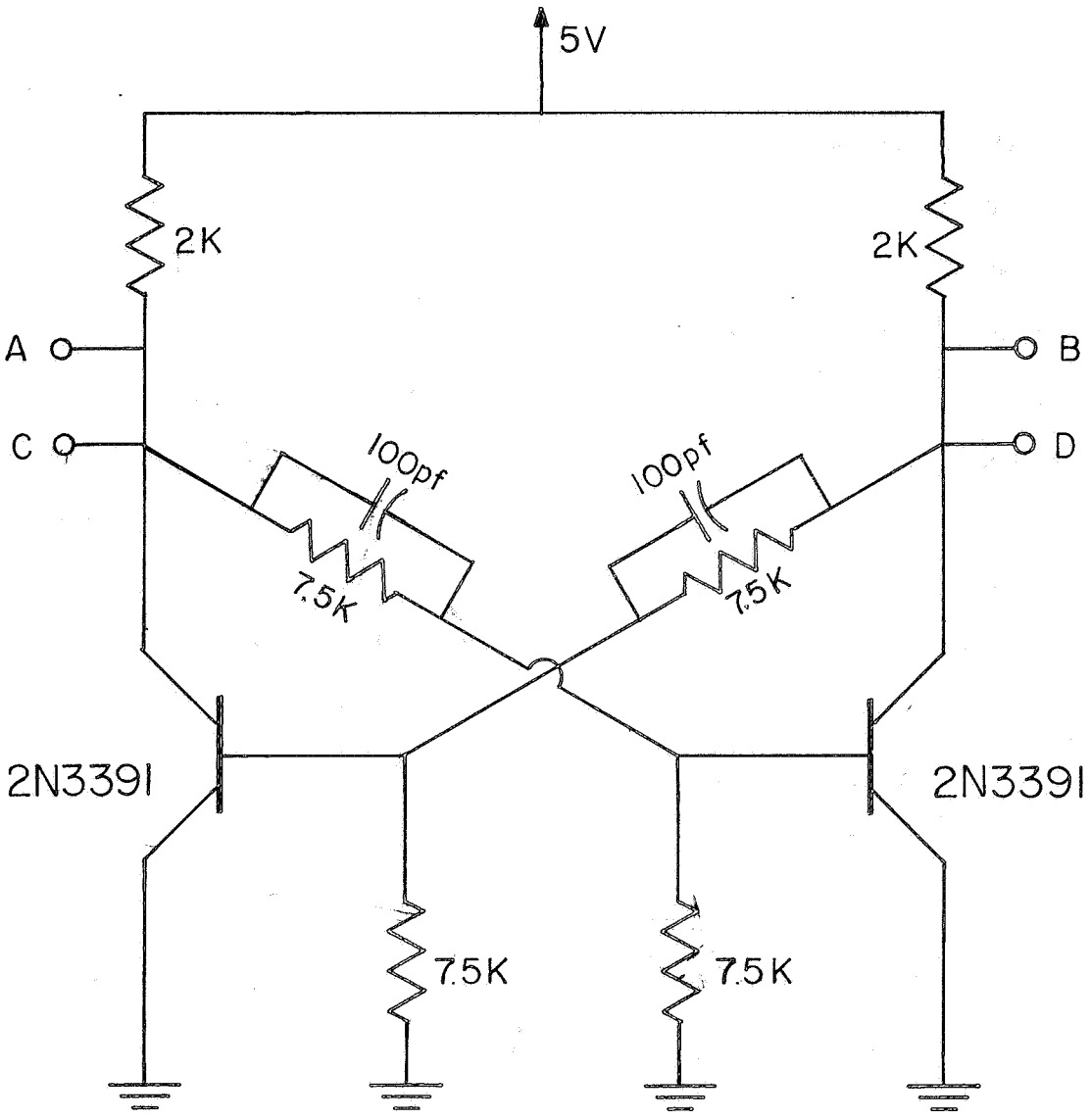


Figure 7. Flip-Flop Used in Setting of Clock (see also FF_1 and FF_2 in Figure 6)

2. Push and release the SET button. This makes

$$A_1 = 1, \quad A_2 = 0, \quad B_2 = 1$$

When the SET button is pushed, the 1 Hz stops and a 10 kHz signal feeds the counters V through W. Since $B_2 = 1$, dividers 1 through 5 are set to zero.

3. When the set time coincides with the indicated time, the output of NAND gate 1 is logic 0 ($A_1 = 0$) and the clock stops counting.

4. When the time to which the clock is to be synchronized is reached, push and release the RUN button. By doing this, the clock is synchronized to the desired time. Since $A_2 = 1$, $B_2 = 0$ when the RUN button is pushed, a 1 Hz signal feeds the counters V through W and the clock runs in its normal mode. The maximum time the clock takes to reach the set time is about nine seconds.

IV. ELECTRONIC DESIGN AND CIRCUIT DETAILS

The two types of flip-flops used in the decade counter SN7490N are discussed in IV.1. The operations of the various I.C. (Integrated Circuit) components SN7490N, NLM200 and NLM100 are discussed in IV.2, IV.3 and IV.4. The need for the inverters and the division by 6 are explained in IV.5 and IV.6. The block diagrams and the different power supplies used are discussed in IV.7 and IV.8. General references for the electronic design are (Hunter, 1962 and Millman and Taub, 1965).

IV.1 Digital Counter Logic (Najjar, 1964)

Six conventional types of memory devices are used in designing digital counters. These are R-S (reset-set), T (trigger), R-S-CP, D (delay type), J-K and J-K-CP flip-flop elements. The BCD decade counters (SN7490N) *used* in the clock's construction are the J-K-CP and R-S-CP flip-flop types (see Figure 8).

IV.1.1 Operation of a R-S-CP Flip-Flop

If it is assumed that Q_t and Q_{t+1} are the states of the R-S-CP flip-flop shown in Figure 8 at two successive time periods t *and* t+1, its properties can be illustrated in binary form shown in Table 2. The first three columns indicate all the possible combinations of states of the inputs R, S and CP at any given time t. The fourth column represents the flip-flop states at bit-time t+1.

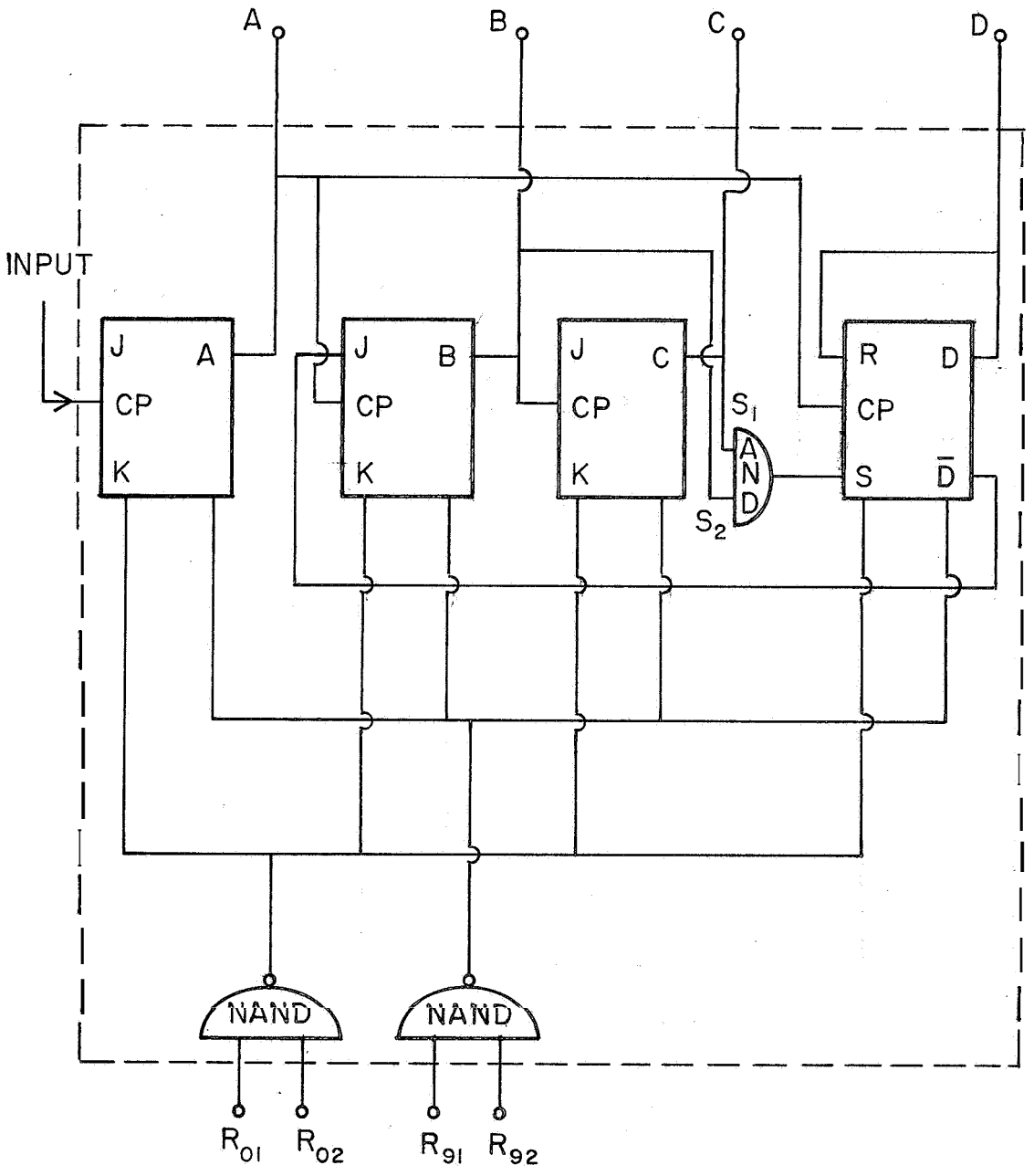


Figure 8. Decade Counter SN7490N

Table a - Logical Properties of R-S-CP Flip-Flops

Bi Time t			Bit Time t+1
R_t	S_t	CP_t	Q_{t+1}
0	0	0	Q_t
0	0	1	Q_t
0	1	0	Q_t
0	1	1	P
1	0	0	Q_t
1	0	1	0
1	1	0	undetermined
1	1	1	undetermined

The logical properties given in Table 2 can be summarized in a Truth Table shown as Table 3.

Table 3 - Truth Table for R-S-CP Flip-Plop Operation

Q_t	Q_{t+1}	R_t	S_t	CP_t
0	0	X	0	X
0	0	0	X	0
0	1	0	1	1
1	0	1	0	1
1	1	0	X	X

X indicates either logic 1 or 0

From Table 3 the logical properties of R-S-CP flipflop can be expressed by the following Boolean equations,

$$Q_{t+1} = \bar{R}_t Q_t + CP_t S_t \bar{R}_t$$

and

$$R_t S_t = 0$$

IV.1.2 J-K-CP Flip-Flop

The J-K-CP flip-flop has three input terminals J, K and CP (clocked pulse). The outputs of the FF are level outputs. The output state Q_{t+1} for all combinations of inputs are tabulated in Table 4.

Tabla 4 - Logical Properties of J-K-CP Flip-Flop

Bit Time t			Bit Time t+E
J_t	K_t	CP_t	Q_{t+1}
0	0	0	Q_t
0	0	1	Q_t
0	1	0	Q_t
0	1	1	0
1	0	0	Q_t
1	0	1	1
1	1	1	$\bar{Q}_t$

In order to determine the input conditions for both J and K in terms of Q_t and Q_{t+1}, it is necessary to proceed in the same way as for R-S-CP flip-flops. The results are presented in the following Truth Table.

Table 5 - Truth Table for J-K-CP Flip-Flop Operation

Q_t	Q_{t+1}	J_t	K_t	CP_t
0	0	X	X	0
0	0	0	0	X
0	1	1	X	1
1	0	X	1	1
1	1	X	0	X

From Table 5 the characteristic equation for the J-K-CP flip-flop can be written as

$$Q_{t+1} = CP_t J_t \bar{Q}_t + \bar{K}_t Q_t$$

IV.2 Operation of SN7490N Decade Counter

The decade counter can be set externally to desired output levels by assigning proper logic levels, presented in Table 6, to reset inputs R_{01}, R_{02}, R_{91} and R_{92}. These are input terminals of the two NAND gates and have been shown in Figure 8. For counting, R_{91} and R_{92} are grounded, R_{02} is connected to V_{cc} and R_{01} is connected to B_2. The CP input of J-K-CP and R-S-CP flip-flops used in the counter SN7490N are sensitive only to negative steps.

In Figure 8 A, B, C and D are level outputs of the counter. Output A drives the CP input of the second J-K-CP flip-flop and the CP input of R-S-CP flip-flop; output $\bar{D}$ drives the J input of second J-K-CP flip-flop; output B drives the CP input of the third J-K-CP flip-flop. With R = D and S = $S_1 S_2$ = BC, the J's and K's of first *and* third FF's are maintained at logic 1 whereas

Table 6 - Reset/Count

Reset Inputs				Output			
R_{01}	R_{02}	R_{91}	R_{92}	D	C	B	A
1	1	0	X	0	0	0	0
1	b	X	0	0	0	0	0
X	0	1	1	1	0	0	1
0	X	1	B	1	0	0	1
1	1	1	E	1	0	0	1
X	0	X	0	count			
0	X	0	X	count			
0	X	X	0	count			
X	0	0	X	count			

$J = \overline{D}$ and K is maintained at logic 1 for second FF. The logic operation of the decade counter for ten input pulses is shown in Table 7.

At the first pulse, the second FF cannot respond since A is a positive step. At the second pulse, the second FF responds to a negative step at its CP input and $J = \overline{D} = 1$. At the fourth pulse, the third FF responds to a negative step and its CP input since its CP = B. At the end of the seventh pulse, the fourth FF's input states are S = 1 and R = 0. At the eighth pulse the fourth FF responds to a negative step at its CP and sets D to 1. At the tenth pulse, the fourth FF responds to the negative step at its CP and sets D = 0. Since there is a negative step at the CP input of the second FF, it can set B to 1 if its J input is one. But by the time $\overline{D} = 1 = J$, there is

Table 7 - Logic Operation of Decade Counter

	Binary Outputs					
Input Pulse	D	C	B	A	S	$\overline{D}$
0	0	0	0	0	0	1
1	0	0	0	1	0	1
2	0	0	1	0	0	1
3	0	0	1	1	0	1
4	0	1	0	0	0	1
5	0	1	0	1	0	1
6	0	1	1	0	1	1
7	0	1	1	1	1	1
8	1	0	0	0	0	0
9	1	0	0	1	0	0
10	0	0	0	0	0	1

no longer a negative step at CP of the second FF. So B remains equal to 0. We then have A = 0, B = 0, C = 0, D = 0 and the counter is ready to start the next cycle of counting. Figure 9a shows the output wave forms at A, B, C and D for a count input of 10.

IV.3 Operation of NL-M200 Readout Tube Decimal Counter/Driver

The decimal numbers can be expressed in terms of the binary outputs in the following way:

Decimal Number	Binary Outputs
0	$\overline{8}\ \overline{4}\ \overline{2}\ \overline{1}$
1	$\overline{8}\ \overline{4}\ \overline{2}\ 1$

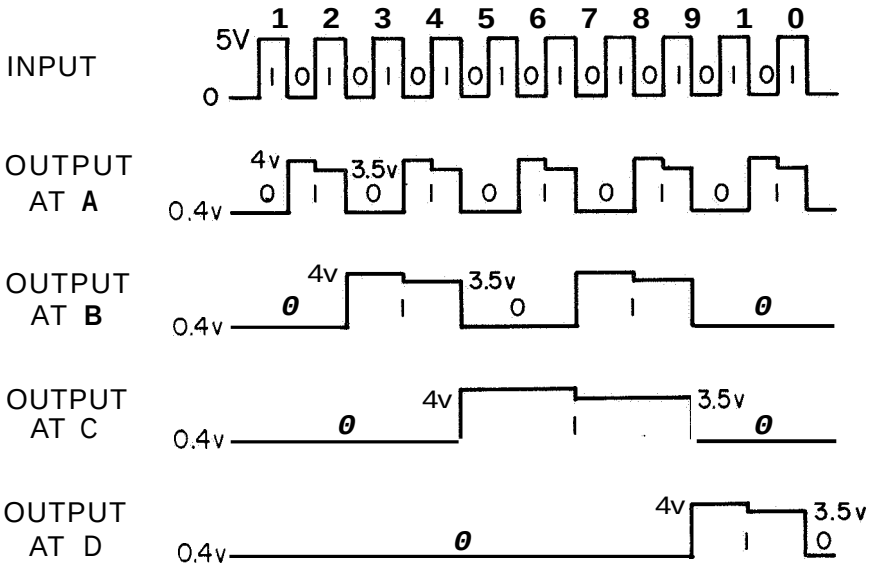


Figure 9a. Output Wave Forms of the Decade Counter

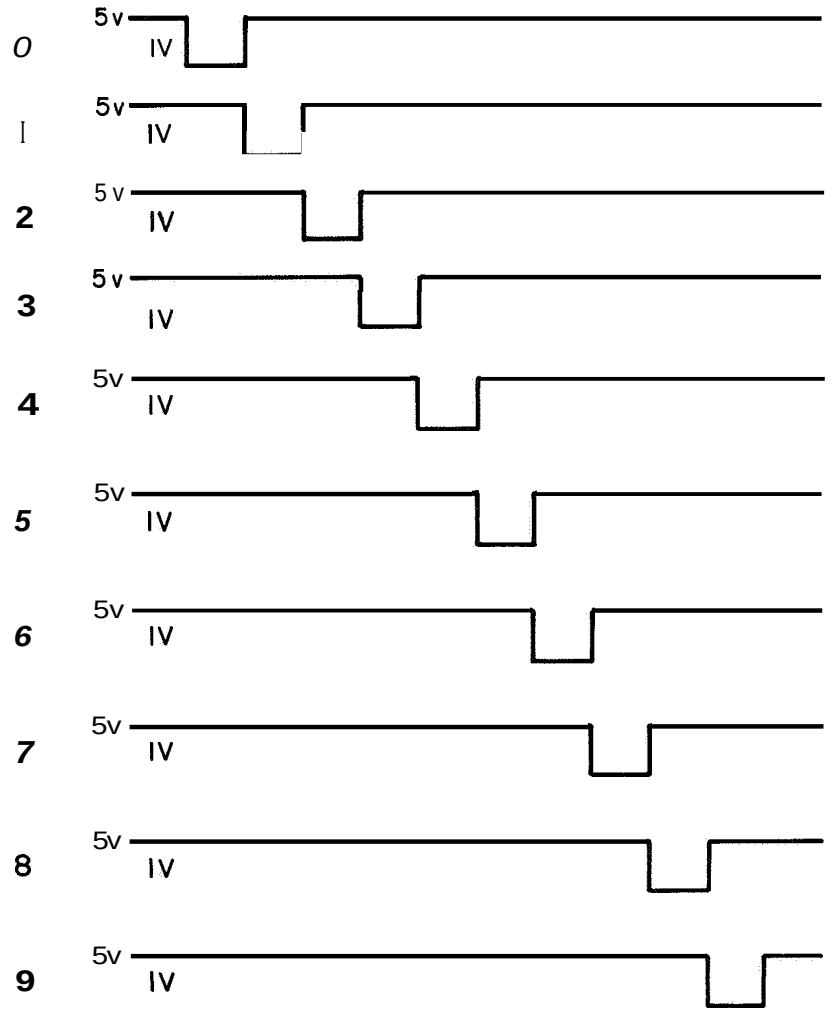


Figure 9b. Output **Wave Forms of the Binary to Decimal Decoder**

2	$\overline{8}\ \overline{4}\ 2\ \overline{1}$
3	$\overline{8}\ \overline{4}\ 2\ 1$
4	$\overline{8}\ 4\ \overline{2}\ \overline{1}$
5	$\overline{8}\ 4\ \overline{2}\ 1$
6	$\overline{8}\ 4\ 2\ \overline{1}$
7	$\overline{8}\ 4\ 2\ 1$
8	$8\ \overline{4}\ \overline{2}\ \overline{1}$
9	$8\ \overline{4}\ \overline{2}\ 1$

where 8, 4, 2 and 1 ($\overline{8}$, $\overline{4}$, $\overline{2}$, $\overline{1}$) are binary outputs (complements) of the decimal counter. The binary outputs become inputs to the respective transistors, as shown in Figure 10, Corresponding to the decimal number satisfying the above table. The transistors conduct only when the voltage equivalent to logic 1 is present at each of its four inputs. The collector of each transistor is connected to the respective cathode of the readout tube.

The readout tube is a gas filled, cold cathode diode with multiple cathodes. Each cathode is shaped as a display character (decimal number) and has a separate base pin electrical connection. When the transistor conducts, the corresponding decimal. number has a path to ground and this causes the shaped glow discharge. The "on" transistor is operated in saturation and the "off" transistors are operated in a back bias state.

IV.4 NL-M100 Decoder/Driver

The NL-M100 decoder/driver is used in parallel with the decoder driver of NL-M200 to generate a decimal output. NL-M100 is similar to the NL-M200 except that the decimal counter and the readout tube are not present. Since E_{bb} is not needed in this case (no readout tube), V_{cc} is applied through a

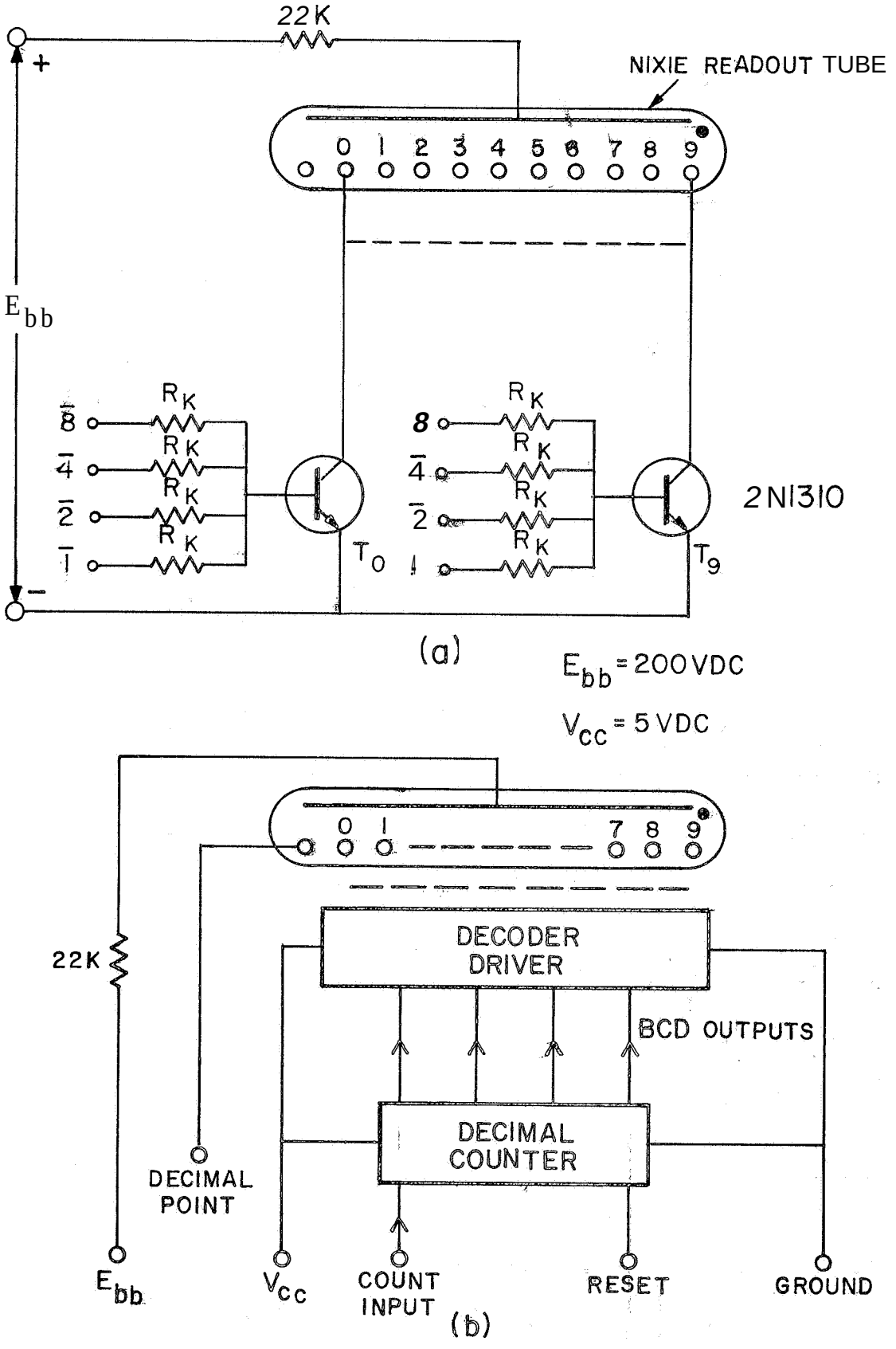


Figure 10. NL-M200 Readout Tube **Decimal** Counter/Driver

load resistor R_L to the collector of each transistor as shown in Figure 11. When a logic 1 is present at each of the inputs of the transistor, the transistor conducts and the output is shown in Figure 9b. (Note that logic levels are inverted.)

IV.5 Inverters

To have compatible positive logic for the gates,, the decimal output must be inverted from plus five volts to zero volts and from plus one volt to plus five volts. This is accomplished by using the inverter shown in Figure 12. The resistors are all 1/4 watt and have a 5% tolerance.

IV.6 Division by Six

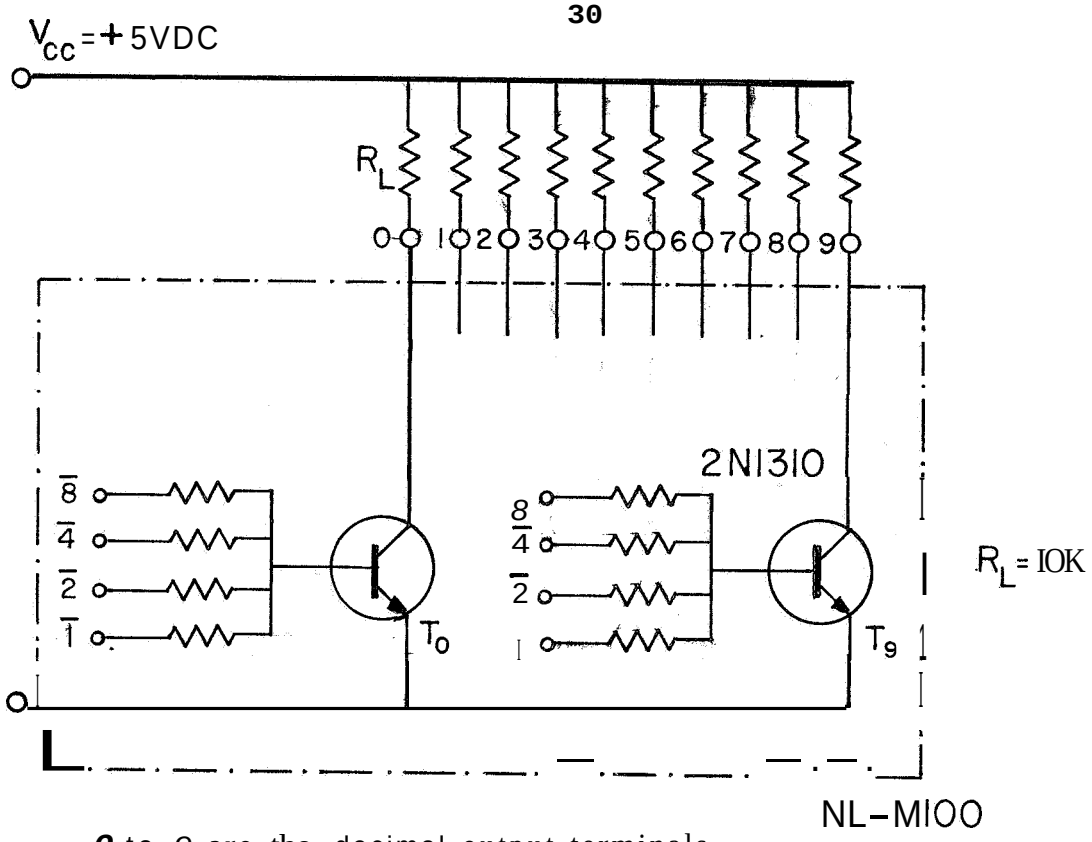
To have the clock read in hours, minutes and seconds, a division by six is needed. This division can be accomplished two ways. These are discussed in the following subsections.

IV.6.1 By Using AND Gate

The 1/10 seconds counter U should reset all of its binary outputs to zero at the sixth input-pulse, and the nixie should change from 5 to 0 without indicating six. This can be accomplished by using an AND gate indicated in Figure 5 and connected as shown in Figure 13, At the sixth incoming pulse, there are level outputs at B and C. Using the AND gate as shown, the BCD counter will be reset to zero at the sixth pulse. The output of AND gate resets U to zero and drives the succeeding Z counter.

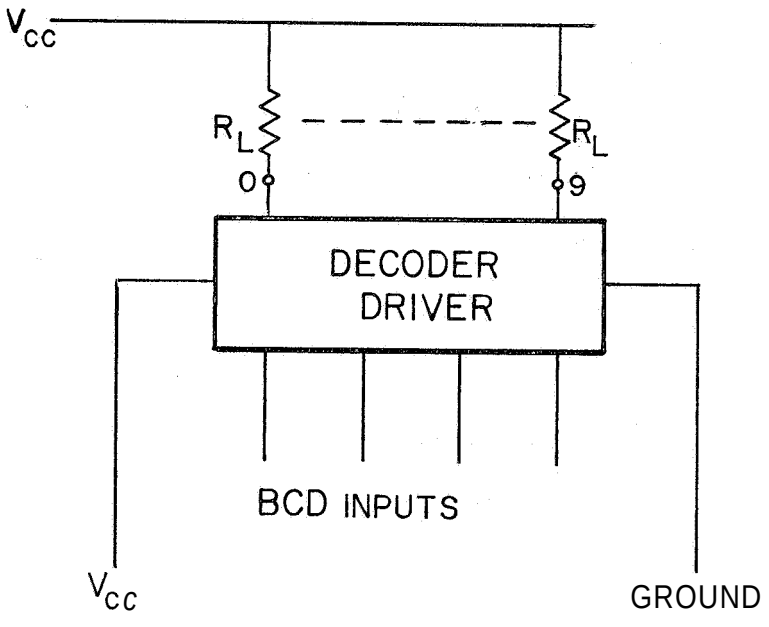
IV.6.2 By Using Decoder Output

The 1/10 minutes counter Y also must be reset to zero at the sixth pulse. In this case since the decimal output of counter Y is available from its



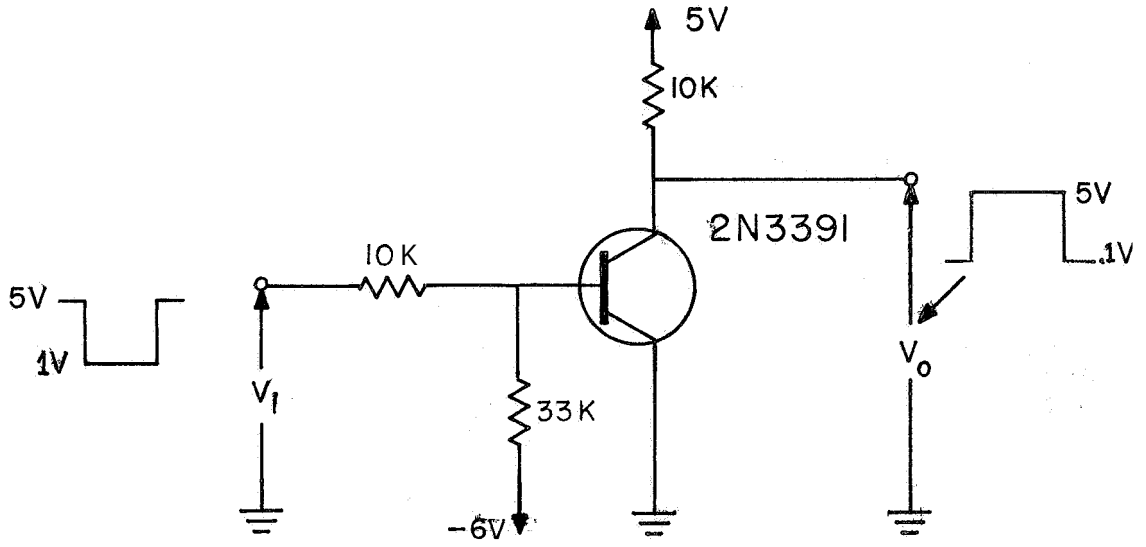
0 to **9** are the decimal output terminals.

(a)



(b)

Figure 11. NL-M100 Decoder/Driver



V_i = Input Pulse (i^{th} decimal output of decoder

V_o = Output Pulse

Figure 12. Inverter

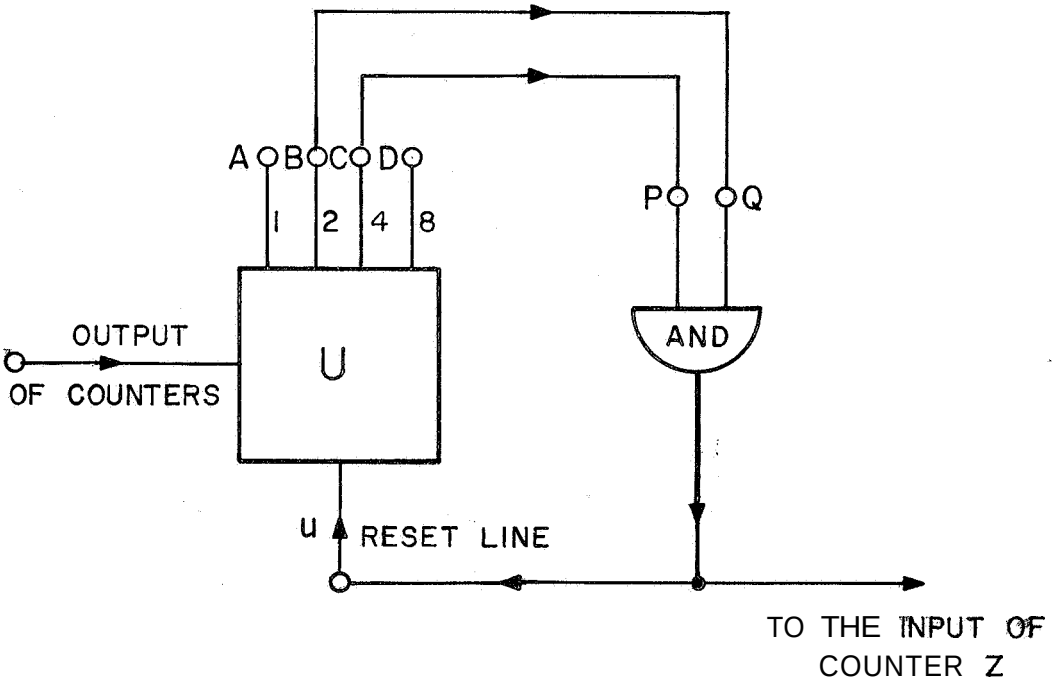


Figure **13. Division by Six Using an AND** Gate

decoder, the counter can be reset to zero using this decimal output (See Figure 14). The decimal output 6 of the Y decoder is fed to the reset input of Y and to the succeeding X counter.

There will be a time delay of about 40n secs in both cases before the counters change from 6 to 0. The nixie cannot respond during this time, and one can only see it changing from 5 to 0.

IV.7 Block Diagrams

The detailed block diagrams of the clock are shown in Figures 15 and 16. Note that four rotary switches are used for each ON setting. The switched contacts are wired in parallel and each wiper contact is connected to a NAND gate input. The operation of the clock is discussed in V.

IV.8 Power Supplies

The schematic diagrams of the +5v DC, +200v DC and -6v DC power supplies are given in Figures 17 and 18.

The five volt supply is an Acopian Model 5A201 regulated power supply with a line regulation of $\pm$0.5%, load regulation of $\pm$0.5%, maximum output load current of 2.1 amperes and an RMS ripple of 5 mv.

The two hundred volt supply for the nixie readout tubes is a zener diode regulared supply. The output of a full wave bridge rectifier is filtered with a RC pi filter and then connected to a 200v zener diode through a current limiting resistor. Since the nixi voltage is not critical (200 $\pm$ 10%), regulation by the zener diode is more than adequate.

The minus six volt supply is a standard transistorized regulared supply. This design has been used many times in other equipment at the Geophysical

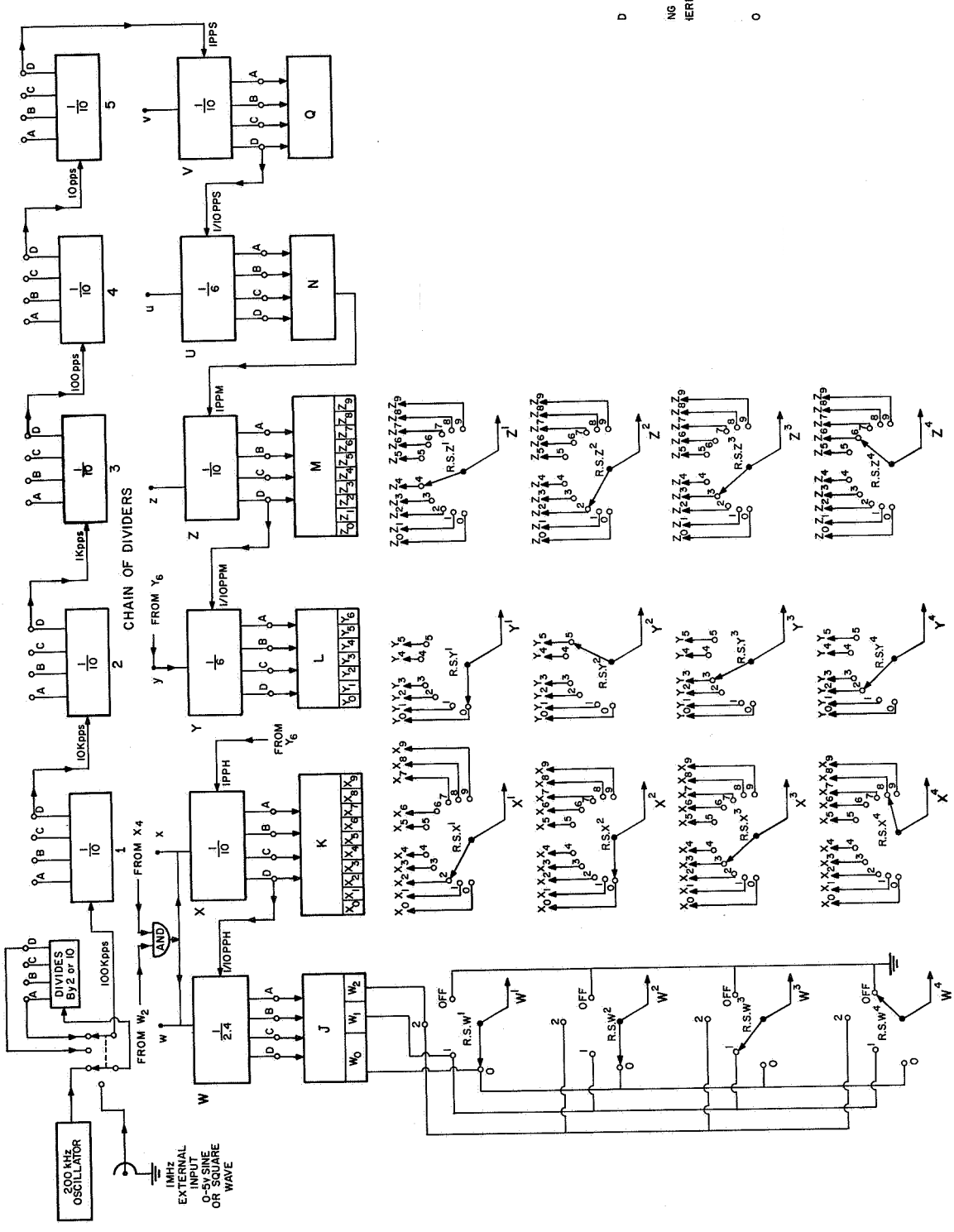
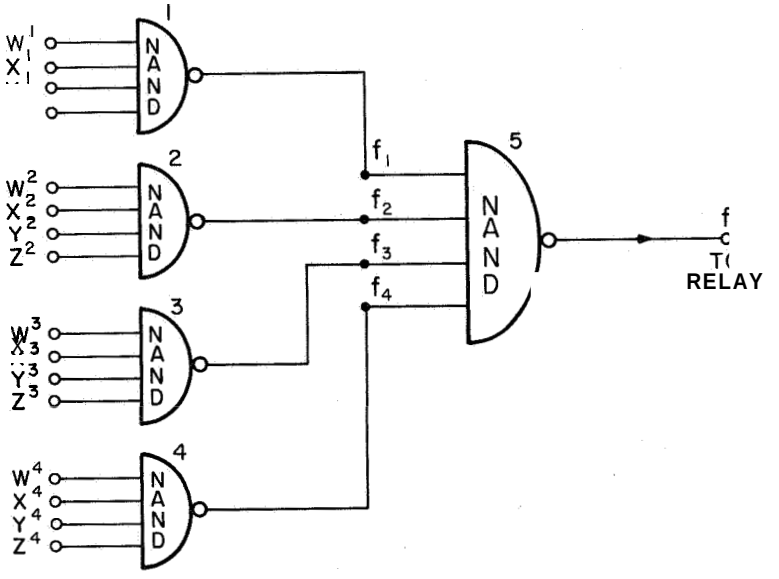
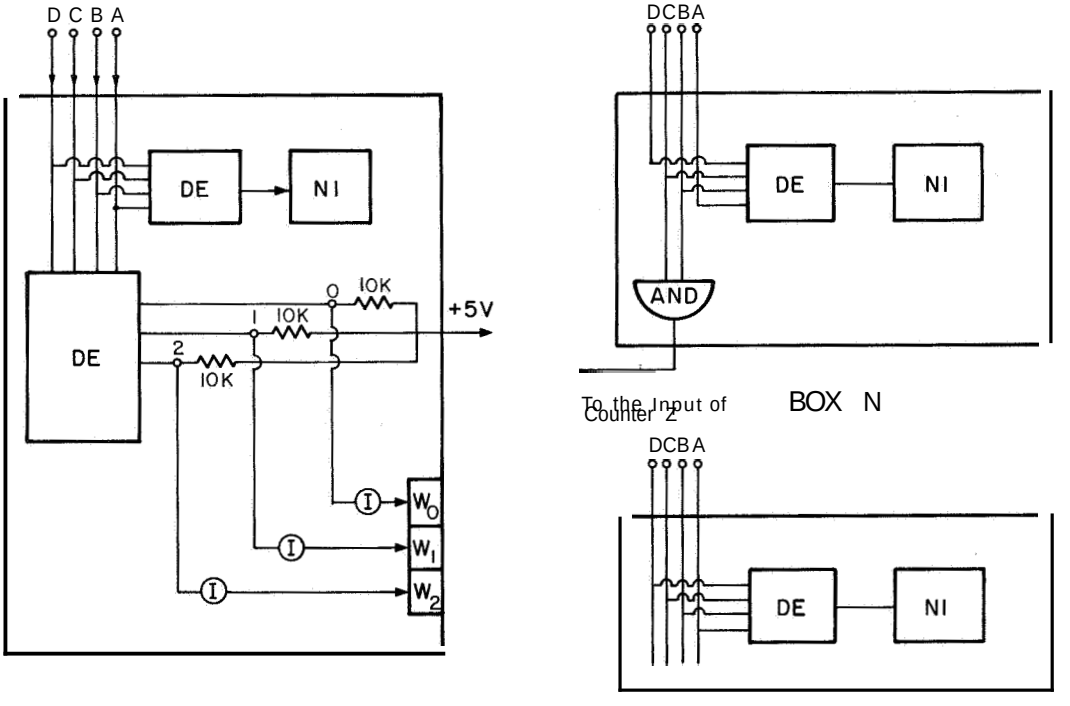


Figure 15. Digital Clock Block Diagrams with Preset Switches (see also Figure 16)

LOGIC



CONTENTS OF BOXES J, K, L, M, N, Q,



BOX J

BOX N

BOX Q

NOTES:

1. Boxes K, L, M Are Similar to **Box** J Except that They Have Different Number of Decimal **Outputs As** Shown in Diagram 4
2. DE — Binary to Decimal Decoder
3. NI → Nixie Readout Tube
4. (I) → Inverter

Figure 16. Detailed Block Diagrams of the Preset Logic and of the Decoders (see also Figure 15)

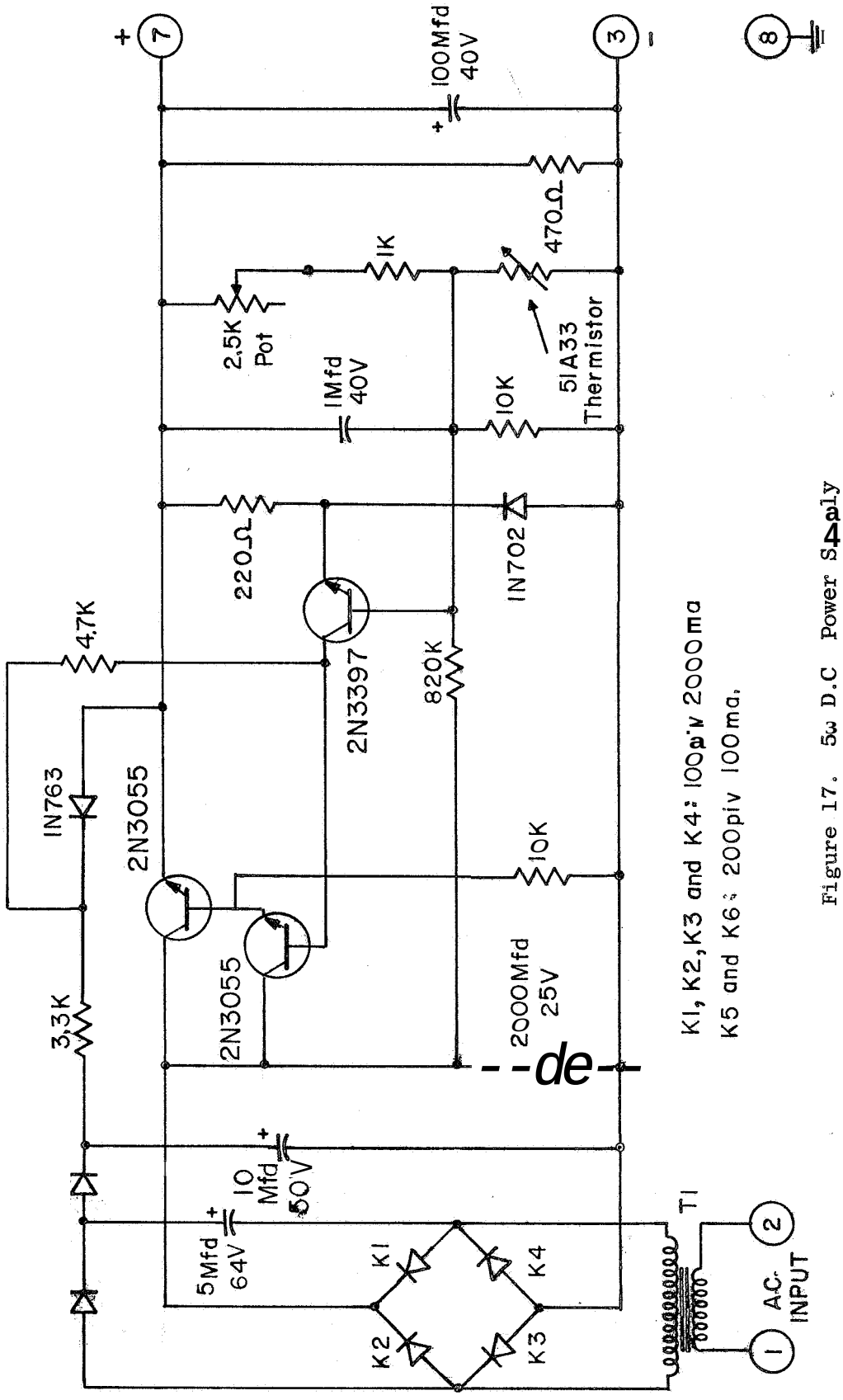


Figure 17. 5w D.C Power Supply

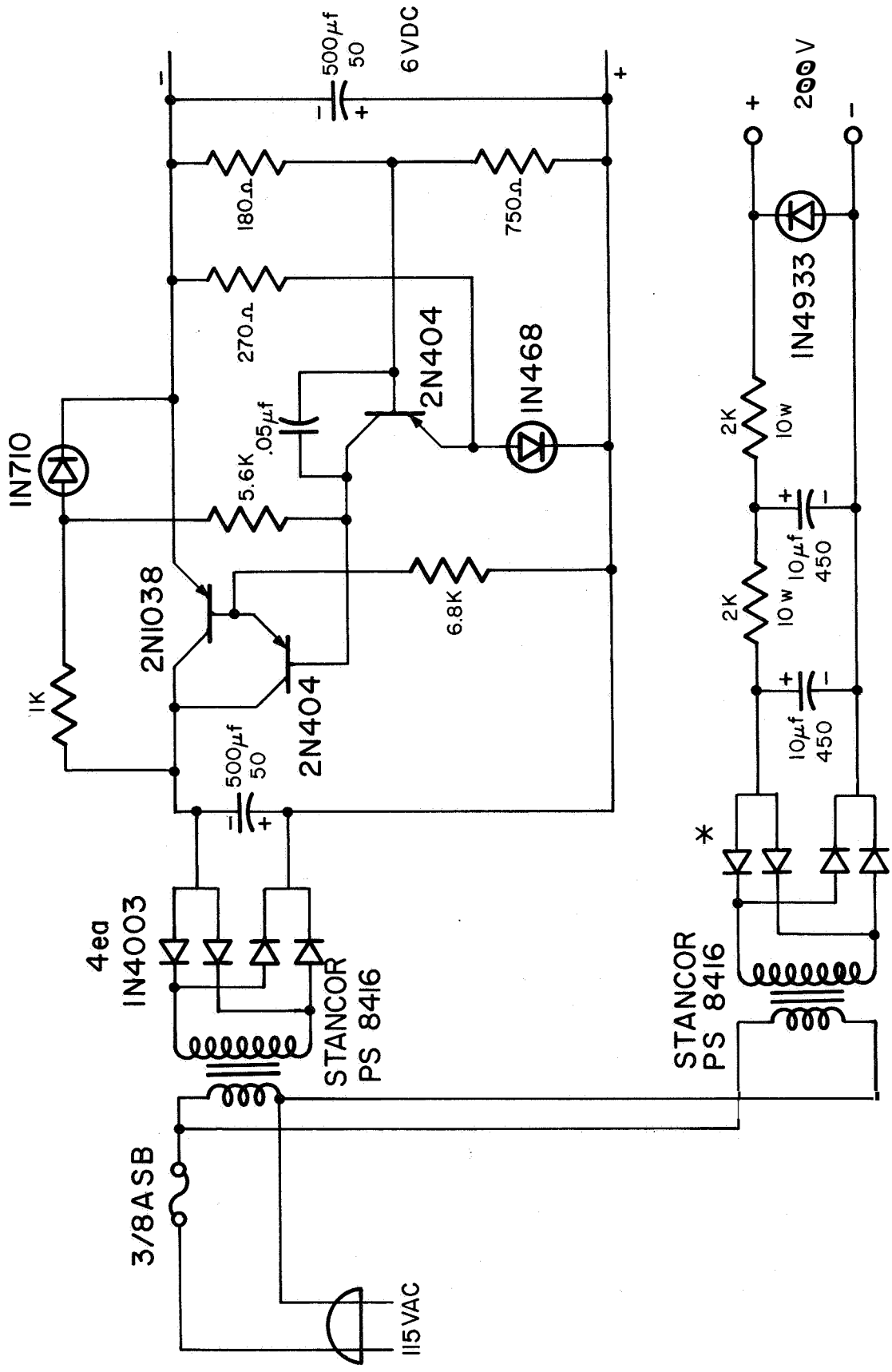


Figure 18 200w D C Power Supply for the -6w D.C Power Supply

Observatory. Line, Load and ripple specifications are similar to those of the plus five volt supply except the maximum current is 100 ma.

V. OPERATION OF THE CLOCK

The given 100 KHz supply frequency is counted down to 1 Hz by using five SN7490N decade counters in cascade, Figures 6, 15 and 16 describe the clock in detail.

W, X, Y, Z, U and V are the decade counters (SN7490N) that drive the BCD to decimal decoder/driver and the nixie indicator, A BCD-to-decimal decoder/driver is connected in parallel with the other decoder/driver for counters W, X, Y and Z. The decimal outputs of the decoder are shown in Figure 9b. Since these outputs are inverted with respect to the standard logic levels, each decimal output drives an inverter (Figure 12). The decimal outputs from the inverters of each counter are connected *in* parallel to the four rotary switches corresponding to the four ON settings. The line selecting terminal of each rotary switch corresponding to the pth decoder (p = W, X, Y and Z) and the nth OM setting (n = 1, 2, 3 and 4) goes to the nth NAND gate. When the nth ON setting (n = i) coincides with the indicated time, the output f_i is 0, and the outputs of the remaining NAND gates, $f_{n\neq i}$, n = 1, 2, 3, 4 are one, f_1, f_2, f_3 and f_4 are the inputs to NAND gate five. At the ith setting, $f_i = 0$ and $f_{n\neq i} = 1$, n = 1, 2, 3, 4. Therefore f = 1, which operates the relay to record the data.

The operation *of the* clock has to be independent of the number of ON settings that are being used at a time, To achieve this, each ten hour rotary switch is provided with a ground point. If any of the four ON settings are not required, the corresponding ten hour rotary switches should be kept at the OFF position (ground point).

The setting of the clock and its automatic change from 2359:59 to 0000:00 are explained under the respective titles.

The digital clock with four ON settings has been built and is working to the desired specifications. Some of the salient features of the clock are discussed in the next section.

VI. SALIENT FEATURES OF THE DIGITAL CLOCK

1. The switches corresponding to the first of the four ON settings are used to set the clock. Since the synchronization of the clock to a given time is accomplished manually by pushing a button, an inaccuracy, depending upon how well one can synchronize, is introduced in the indicated time. If higher accuracy of the indicated time is required, electronic rather then manual synchronization is recommended. This can be accomplished by using a pulse generated from WWV, or other suitable source, to turn on a transistor. The transistor would provide the ground path to replace the push button.
2. If more ON settings are required, a NAND gate with inputs equal to the number of ON settings is needed. The maximum number of possible ON settings is sixty, The limiting factor is the collector current, I_c, of the inverter transistor (2N3391). The I_{CMAX} of the 2N3391 is 100 ma. At logic 0 the maximum current from the NAND gates (SN744N) is 1.6 ma. The number of ON settings, N, is determined by the following equation.

$$I_{CMAX} = \text{(inverter load current)} + \text{(gates current)} + \text{(gate current for time change 2359:59 to 0000:00)}$$

$$I_{CMAX} = \frac{(V_{cc})_{MAX}}{(R_L)_{MIN}} + nI_L + \frac{(V_{cc})_{MAX}}{(R)_{MIN}}$$

$$100 \text{ ma} = \frac{5 \times 1.05}{0.95 \times 10K} + 1.6n + \frac{5 \times 1.05}{0.95 \times 2K}$$

$$n = 60$$

3. In the event of a power failure of one-third of a second or longer, all logic is lost and the clock will reset itself to the time set on the first ON setting. The indicated time on the clock will be in error. To prevent this difficulty, it is advisable to run the clock on batteries charged by the line supply.
4. The accuracy of the clock's indicated time is limited by the oscillator accuracy and stability. Long term frequency stability of the 200 KHz oscillator is $\pm 1 \times 10^{-6}$ per day. If better stability is required, the clock is provided with a 1 MHz external input, The input must be 0 to +5 volts positive pulse or a 5 volt peak-to-peak sine wave biased to a plus 2.5 volts.
5. The total power consumption of the digital clock is approximately 10 watts.

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